D. REMARKS

Status of the Claims

Claims 1-21 are currently present in the Application, and claims 1, 8, and 15 are independent claims. Claims 1, 8, and 15 have been amended, no claims have been cancelled, and no claims have been added.

Examiner Interview

Applicants note with appreciation the telephonic interview conducted between Applicants' representative and the Examiner on May 22, 2006. During the telephonic interview, the Examiner and Applicants' representative discussed the 102 reference (Wang et al., U.S. Patent No. 6,981,073). In particular, Applicants' representative discussed that Applicants' invention waits to send an interrupt request, which is generated by a source device and targeted for a destination device, until corresponding data is sent from the source device to the destination device. Applicants' invention ensures that once the destination device receives the interrupt request, the corresponding data is already available and ready to process, which is different than existing art. In contrast, Wang discloses a method to generate an interrupt request that is sent to a controller to clear particular signals. Applicants' representative suggested amending Applicants' independent claims to distinctly claim that the interrupt request corresponds to the data that is sent to the destination device. No agreement was reached regarding the claims.

Title

Applicants have amended the title of the invention in order to more clearly describe the invention, and therefore,

Applicants respectfully request that the Examiner remove the objection to the Title.

Drawings

Applicants note with appreciation the Examiner's acceptance of Applicants' formal drawings filed concurrently with the application.

Claim Rejections - Alleged Anticipation Under 35 U.S.C. § 102(e)

Claims 1-21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Wang et al. (U.S. Patent No. 6,981,073, hereinafter "Wang"). Applicants respectfully traverse these rejections.

Applicants have amended claim 1 to distinctly claim that Applicants' invention sends an interrupt request from a source device to a destination device after the destination device has received corresponding data, and that the interrupt request corresponds to the data. Applicants' claim 1 as amended include the limitations of:

- receiving data at a bridge controller from a source device for a destination device;
- receiving an interrupt request at the bridge controller from the source device for the destination device, the interrupt request corresponding to the received data;
- transferring the data from the bridge controller to the destination device; and
- in response to completing the transferring of the data, forwarding the received interrupt request from the bridge controller to the destination device.

Applicants' invention receives data and a corresponding interrupt request from a source device, both of which are

targeted for a destination device. Applicants' invention then 1) transfers the data to the destination device, and 2) AFTER transferring the data to the destination device, forwards the source device's interrupt request to the destination device. Applicants' invention solves an issue that the prior art creates in that the prior art sends an interrupt request to a destination device before all of the data is ready for the destination device to process the interrupt request. As a result, the destination device has to wait for the data before it processes the interrupt using the prior art. Applicants' invention, however, ensures that all of the data is sent to the destination device BEFORE sending the interrupt request.

In contrast, Wang does not teach Applicants' claim 1 limitations, but rather teaches that a controller tracks a data transfer and generates an interrupt request once a data transfer is complete, which is used by the controller to reset particular signals. Specifically, Wang states:

> "In one embodiment, controller 30a is capable of **generating** an interrupt request (int_dma) signal 62 when a data transfer is completed." (col. 13, lines 3-5)

> "Fig. 20 is a timing diagram of the end of a READ transfer. When the READ transfer is completed, the Valid_xfr_rd signal goes low, and the interrupt dma (int_dma) signal goes high, unless a mask of the interrupt request is activated. The **bus and interrupt controller 26 writes an interrupt command to the controller 30a to reset the signal**, as discussed in Table 5 with IF bit of the status indication register." (col. 26, lines 23-29)

As can be seen from the above excerpts, Wang does not teach "***in response to completing the transferring of the data, forwarding the received interrupt request*** *from the bridge controller to the* ***destination device***" as claimed by Applicants.

First of all, Wang teaches that the controller generates the interrupt request, which is different than forwarding an interrupt request, which was previously received from a source device, as claimed by Applicants. Second of all, Wang sends the interrupt request to the controller, which is different than sending the interrupt request to the destination device as claimed by Applicants.

Therefore, since Wang does not teach all the limitations included in Applicants' claim 1 as amended, amended claim 1 is allowable over Wang. Claim 8 is an apparatus claim including the same limitations of claim 1 and, therefore, is allowable for the same reasons as claim 1 is allowable. Claim 15 is a computer program product claim including the same limitations of claim 1 and, therefore, is allowable for the same reasons as claim 1 is allowable.

Notwithstanding the fact that claim 3 is indirectly dependent upon claim 1 and, therefore, allowable for the same reasons as claim 1 discussed above, claim 3 adds limitations (including claim 2's limitations that claim 3 depends) to claim 1 of:

- storing the **data** in a data queue after the receiving the data; and
- determining and storing in the data queue a **device ID of the source device** and an **address of the destination device.**

Applicants' invention stores 1) data, 2) a source device ID, and 3) a destination device address in a single data queue (refer to Applicants' Figure 2, element 210). The Office Action

cites excerpts in Wang to reject Applicants' claim 3 limitations. After closer review, however, Wang's excerpts do not disclose that all three of the above items (data, source ID, and destination address) are stored in the same data queue.

First, Wang's Figure 4, element 36 is a destination device, which does not store the source device ID. Second, Wang's col. 6, lines 55-56 disclose a device buffer interface unit, but do not disclose that the data, source ID, and destination address are stored in a single data queue. Third, Wang's col. 13, lines 9-11 disclose signal generation, but do not disclose that the data, source ID, and destination address are stored in a single data queue. And fourth, Wang's Figure 11, element 198a is an address generator, which does not store the data as claimed by Applicants.

Therefore, since Wang does not teach all the limitations included in Applicants' claim 3, claim 3 is allowable over Wang. Claim 10 is an apparatus claim including the same limitations of claim 3 and, therefore, is allowable for the same reasons as claim 3 is allowable. Claim 17 is computer program product claim including the same limitations of claim 3 and, therefore, is allowable for the same reasons as claim 3 is allowable.

Notwithstanding the fact that claim 6 is indirectly dependent upon claim 1 and, therefore, allowable for the same reasons as claim 1 discussed above, claim 6 adds limitations (including claim 5's limitations that claim 6 depends) to claim 1 of:

- storing the interrupt request in an interrupt queue after the receiving the interrupt request; and

- determining and storing in the interrupt queue a device ID of the source device and an address of the destination device.

Applicants' invention stores 1) an interrupt request, 2) a source device ID, and 3) a destination device address in a single interrupt queue (refer to Applicants' Figure 2, element 215). The Office Action cites the same excerpts in Wang to reject Applicants' claim 6 as the Office Action used to reject Applicants' claim 3 discussed above. Again, Wang's excerpts do not teach or suggest, in whole or in part, storing each of an interrupt request, a source ID, and a destination device address in a single interrupt queue as claimed by Applicants.

Therefore, since Wang does not teach all the limitations included in Applicants' claim 6, claim 6 is allowable over Wang. Claim 13 is an apparatus claim including the same limitations of claim 6 and, therefore, is allowable for the same reasons as claim 6 is allowable. Claim 20 is a computer program product claim including the same limitations of claim 6 and, therefore, is allowable for the same reasons as claim 6 is allowable.

Each of the remaining claims 2, 4-5, 7, 9, 11-12, 14, 16, 18-19, and 21 each depend, directly or indirectly, upon one of the allowable independent claims 1, 8, and 15. Therefore, claims 2, 4-5, 7, 9, 11-12, 14, 16, 18-19, and 21 are each allowable for the same reasons as their respective independent claims.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition

for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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